

Summary Descriptions of Projects, 2009-2010

CMOS PA and Oscillator Circuits Using Slow-Wave TL's for Communications, Radar and Imaging Applications

David Allstot (University of Washington)

Abstract - Continued scaling of CMOS has allowed for circuit design in frequency bands traditionally only occupied by SiGe and IIIV compounds. Though CMOS circuits have been demonstrated at frequencies in excess of 100 GHz, their performance is not optimal for high-speed communications, radar or medical imaging, due to relatively poor noise performance of oscillators and amplifiers, and low gain in amplifiers. Recent research on slow wave coplanar wave guides (SWCPWG) has demonstrated quality factors in excess of 60, for frequencies in excess of 20 GHz. These SWCPWG structures can be leveraged to produce high quality resonant circuits to enhance the phase noise performance in oscillators operating at microwave frequency. Additionally, due to the low loss characteristics, the structures offer an excellent candidate for power combining networks that can be used to improve gain, output power and efficiency of PAs operating at these frequencies.

Design Automation Techniques for Minimizing Dynamic and Static Energy consumption in Multicore and Mixed-Signal, Wireless Sensor Systems

Patrick Yin Chiang (Oregon State University)

Abstract - Power consumption and energy efficiency are critical requirements for future microelectronics. These considerations are essential for both ends of the technology spectrum – from high-end, multi-gigahertz, multicore computing that are used in cloud-computing servers, to energy-scavenging, sub-threshold operation, wireless sensor SoCs. In order to reduce both dynamic and static power consumption, two methods are typically used: 1) low-voltage swing during normal operation (dynamic); 2) power-gating, block shut-down (static). While there has been an enormous amount of recent work in this ultra-low power arena (sub-threshold digital blocks: D. Blauuw, A. Chandrakasan; power gating optimizations: K. Roy; low-power analog components: T. Fiez, G. Temes, P. Chiang), design automation and the ability to automate these new methodologies into standard mixed-signal flows with minimal design time, reliability, and testability is still severely lacking. We propose in this work new design-automation techniques for implementing low-voltage swing interconnect and power-gating in both multicore and ultra-low power, mixed-signal applications

On-Chip Temperature Sensors and Voltage References for Sub-200 nm CMOS

R. Bruce Darling (University of Washington)

Abstract - The objective of this project is to develop accurate, wide-range, on-chip temperature sensors and voltage references for high-density digital CMOS integrated circuits that are fabricated at the 180 nm node and below. For these newer CMOS processes, many of the traditional approaches to on-chip temperature sensors and voltage references can no longer be applied, and new circuit and device strategies must be developed to sustain the use of mixed-mode data acquisition circuits which are to be embedded within a largely digital system on a chip. On-chip temperature sensing is becoming increasingly important for high-density digital integrated circuits in order to monitor heat loading which may fluctuate wildly with operating conditions and data throughput. The requirements on these temperature sensors include a range of -55°C to $+125^{\circ}\text{C}$ with an absolute accuracy of at least $\pm 1^{\circ}\text{C}$, response times of less than 1 ms, linearity of at least $R2 > 0.9995$ to permit only a 1- or 2-point calibration, small chip area, minimum

power consumption, and a very high power supply rejection ratio (PSRR) of typically 40-50 dB over 100 Hz to 10 MHz to make their use feasible within the high noise environment of a digital IC. This project has emphasized the use of sub-threshold MOSFETs to achieve the exponential current-voltage relationship which can be used as the basis for a proportional-to-absolute-temperature (PTAT) building block. Temperature-controlled oscillators (TCOs) have also been developed as a more compact and more easily interfaced transducer. On-chip voltage references share many of the same features, design constraints, and sub-circuit techniques as on-chip temperature sensors. The classic example of this are bandgap voltage references which utilize a PTAT core. The second objective of this project is to extend the previous temperature sensor techniques to develop on-chip voltage references of about 500-600 mV with temperature coefficients of ~ 20 ppm/ $^{\circ}\text{C}$ over the range of 0°C to $+125^{\circ}\text{C}$ and with PSRRs of at least 40 dB over 100 Hz to 10 MHz. Both the temperature sensors and voltage references are being developed to operate over a range of power supply voltages from 1.8 V down to 1.0 V and below.

Low-Power Low-Jitter All-Digital Frequency Synthesizers

Pavan Kumar Hanumolu (Oregon State University)

Abstract - The goal of our proposed research is to explore and invent system- and circuit-level design techniques that will enable ultra low-power clock generators. Particular emphasis is on the implementation of digital frequency synthesizers that have high excellent jitter performance over a wide operating range and have excellent immunity to supply noise at all frequencies. To this end we propose: (a) a digital multiplying delay-locked loop architecture, (b) a novel replica-based regulator that improves the supply noise rejection ratio of a conventional regulator by 60dB and, (c) a digital supply noise cancellation scheme. With the aid of the proposed techniques we seek to achieve better than 2% long-term r.m.s jitter with better than 0.25mW/GHz power efficiency.

Adaptive Body-Enabled Low Power PLL with Wide Locking Range

Deuk Heo (Washington State University)

Abstract - Integrated circuits and systems are driven toward higher operating frequencies and a higher level of integration by the demand for lower power, wider bandwidth and higher data rates in both wired and wireless communication systems. Low power, high linearity and low noise, are significant challenges that need to be addressed for high performance of wired and wireless communication terminals. In our previous CDADIC project, we verified that the body signal, including DC bias and AC coupling signal, enabled by triple-well process, can be optimized to reduce threshold voltage, increase transconductance (gm) and reduce the noise figure of RFICs via innovative body-enabled techniques such as body biasing and body coupling. In addition, voltage controlled oscillators (VCOs) and linear low noise amplifiers (LNAs), as we developed in our previous CDADIC project about adaptive body-enabled technique can be applied to highly linear mixer and wideband LNA for RF front end, as well as fast settling and wide locking range phase-locked loops (PLLs). The objective of this proposal is to investigate adaptive body-enabled low power PLL with wide locking range based on scaled CMOS technology. For the adaptive body-enabled technique, we will mainly focus on the investigation of mixer based phase frequency detectors (PFD), charge pumps with negative feedback to allow the body bias to reduce current mismatch, multi-phase voltage controlled oscillators with adaptive body biasing, and multi-phase injection locked frequency dividers with body coupling, to lower the power consumption and improve their respective performance of PLL.

High-Throughput Data Busses

George La Rue (Washington State University)

Abstract - As CMOS technology continues to scale with higher speed, density and integration levels, input/output (I/O) capacity becomes even more of a bottleneck. With the advent of multi-core processors, I/O bandwidth needs to scale not only with the higher speed of the technology but by an additional factor of the number of cores. Current data rates of a few Gbps are standard and rates are expected to increase

soon to 10 Gbps. This project expands on the investigation of techniques to increase I/O capacity. Currently we are exploring techniques using single-ended signaling to achieve data rates near to that of differential

signaling to increase the I/O capacity by 50% for the same number of I/O pins. We have investigated three methods to allow single-ended signaling to achieve data rates nearly equal to that of differential signaling: reducing power supply bounce by coding across groups of signals, compensating for nearest neighbor crosstalk and providing the equivalent of common mode rejection. Layout of a test chip with a 16-bit single-ended bus in 90 nm technology at 8 Gbps per line is nearing completion. The test chip will be used to demonstrate a throughput of over 120 Gbps over 5 to 10 inches of FR-4 material with 21 I/O pins. The test chip also includes differential I/O structures for comparison. In addition to characterizing the single-ended design this year, we will investigate the implementation of serial links in the 80 Gbps to 150 Gbps range using STMicroelectronics' 65 nm CMOS process. One or two differential links at this high rate provides the same throughput as a 16-bit bus at 8 Gbps. We will investigate not only the circuit design for these higher-speed links but also the packaging and printed circuit board (PCB) requirements for operating at these high rates. Typically at these very high data rates inductors are used in the loads of Common Mode Logic (CML) gates to increase performance. The large layout area of these inductors dominates the design. Extra-delayed-clock (EDC) flip-flops have been shown to improve bipolar CML performance without using inductors although using inductors in conjunction with EDC flip-flops improves performance further. We will investigate the use of FET-based EDC flip-flops in these data links to reduce the use of inductors and save considerable layout area.

Low-Voltage Analog Circuits in CMOS

Un-Ku Moon (Oregon State University)

Abstract - In past years our low-voltage analog circuits research has been focused on highly linear switched filters, mixers and data converters. Circuit advancements from this research include the development of the Switched-R-MOSFET-C (SRMC) filter architecture and downconversion filter architecture. Since the last CDADIC winter meeting we have continued the development of a continuously reconfigurable ADC, which uses switched resistors as a means to achieve high performance continuous tuning. We have also completed work on a hybrid comparator based pipeline ADC. In the next research period we will investigate a low power domino logic based ADC. One of the important goals in this research has been to develop new circuit techniques that would be fully compatible with future state-of-the-art CMOS technologies which is anticipated to operate under very low supply voltages. Our previous CDADIC reports include many detailed discussions regarding various new techniques developed under this project. In the following, we will summarize our progress since our last winter meeting. The contents of this report include implementation details of the reconfigurable ADC. The proposal will conclude with an overview of the proposed domino logic based ADC.

Ultra-Low Power Fully-Integrated MICS-Band Transceiver

Brian Otis (University of Washington)

Abstract - New applications of the Medical Implant Communications Service (MICS) band are rapidly emerging. The need for ubiquitous body area networks (BAN) that continually sense heart rate, blood pressure, glucose, acceleration, and even brain signals is growing along with the aging population. Ultra-low-power radios are an essential component of this vision. Battery replacement for implanted and body-worn devices may not be feasible or desirable, thereby placing extreme requirements on the total power dissipation of the radio transceiver that tends to consume a bulk of the total power. We propose novel transmitter and receiver architectures that will enable a fully-integrated sub-0.5mW end-to-end wireless link, lower than any transceiver reported to date. This project will result in novel transceiver architectures which will advance the state-of-the-art in low power radio design.

Micro-Power Data Converters

Gabor Temes (Oregon State University)

Abstract - The purpose of the proposed research is to develop micro-power data converters, both ADCs and DACs. Such A/D converters are often needed in sensor networks used in environmental monitoring, medical sensors and probes, industrial control, security and other applications where power is provided by batteries or energy scavenging, and hence it is very limited. The micro-power DACs may be used in micro-stimulators and micro-actuators in biomedical applications. The tentative specifications call for a narrow signal band (0 ~ 1 kHz), medium accuracy (12 ~ 14 ENOBs), and the lowest possible power dissipation, ideally only a few microwatts.

Enabling Metal-Fill-Aware Design of RF/Mixed-Signal Integrated Circuits

Andreas Weisshaar (Oregon State University)

Abstract - The objective of this project is to enable metal-fill-aware design of RF/analog and mixed-signal integrated circuits. The approach is to make metal fill cells an inherent part of the design and layout process and develop design guidelines for the placement, shape and size of metal fill cells near passive components and interconnects. A scalable modeling methodology and closed-form expressions for representing the electric parasitic effects of metal fill in terms of effective substrate permittivity parameters are developed. To demonstrate the efficiency and accuracy of the modeling approach, the models are verified with electromagnetic simulations and further validated with measurements. Electromagnetic parasitic effects of metal fill on on-chip transmission line performance are demonstrated through simulation and measurement. The degradation of spiral inductor performance due to metal fill is also demonstrated by measurement results. A simple mitigation technique for reducing these metal fill effects is demonstrated through measurement results. In the next project period, the modeling methodology will be extended to single and coupled interconnects and passive components including spiral inductors and baluns. A test chip with representative test structures will be designed, fabricated and tested to validate the proposed modeling methodology and design guidelines.