

## Summary Descriptions of Projects Funded, 2011-2012

### Variation Resiliency of Digital Circuits Using Analog-Assisted Techniques

*Patrick Yin Chiang (Oregon State University)*

**Abstract** - Digital sub/near-threshold logic has been proposed as approaching the energy-optimal performance, but exhibits two fundamental limitations preventing their widespread adoption: a) low frequency of operation (MHz); b) large timing variations due to process variability. Near-threshold operation exhibits timing delays that are not predictable, and can be prohibitively long. Lower V<sub>dd</sub> means less gate overdrive, meaning gate resistances will be more sensitive to process variations, such as threshold voltage mismatches. For example, in super-threshold, a 13% delay variation may be expected; in sub/near-threshold, delays can vary from 4x-20x. As the number of cores increases, the likelihood of seeing large timing uncertainties will severely limit maximum clock frequencies. Reducing the clock frequency directly increases both the cost and the power, as more cores are needed to satisfy the throughput requirements requiring more area, and dissipating more leakage and communications power overhead. In this proposal, we will explore mixed-signal circuits and systems that can: a) increase the throughput of operating in near-threshold by incorporating computational parallelism; b) novel digital and analog circuits for improving timing variation and reliability at low-V<sub>DD</sub> operation.

### Low-Power Low-Jitter All-Digital Frequency Synthesizers

*Pavan Kumar Hanumolu (Oregon State University)*

**Abstract** - The goal of our proposed research is to explore and invent system-and circuit-level design techniques that will enable ultra low-power clock generators. Particular emphasis is on the implementation of digital frequency synthesizers that have excellent jitter performance over a wide range of reference frequencies. To this end, we propose: (a) a novel digital phase accumulation based PLL architecture and (b) intrinsic oscillator phase noise suppression techniques.

### Highly Linear MMICs for Wideband Beamformer Transmitter Applications

*Deuk Heo (Washington State University)*

**Abstract** - The existing beamforming systems on silicon are mostly narrow band and span only a few bands of interest. Conventional techniques that are applied to improve bandwidth and linearity are not sufficient to meet performance requirements for multi-band operations in the low voltage scaled silicon process. We propose to advance the current state-of-the-art Tx beamforming chip by optimizing the performance of each key sub-block in terms of linearity, bandwidth, and phase accuracy. A single channel transmitter beamformer will be developed which will be easily scalable to multi-channel Tx beamformers. The design of Ku to Ka band MMICs for beamformers is challenging in terms of the wide bandwidth, linearity, and power consumption. In addition, the high frequency devices suffer from model accuracy. Hence, the system architecture of the transmitter beamformer is carefully defined taking into consideration linearity, bandwidth, gain, phase accuracy, power consumption, process invariance and scalability to multi-beam applications. Based on silicon technologies, key sub-blocks including wideband phase shifter, highly linear VGA with reduced phase variation and low complexity

power amplifier will be investigated and implemented. A novel method to enhance bandwidth of quadrature phase shifter is proposed. Novel design methodologies are utilized to enhance bandwidth and linearity and reduce power consumption of VGA and PA.

### High-Speed ADC in Digital CMOS

*George La Rue (Washington State University)*

**Abstract** - A 10 GSps analog-to-digital converter (ADC) architecture that first converts the input voltage to the time domain followed by a time-to-digital converter (TDC) is proposed. The advantage of the analog-to-time-to-digital converter (ATDC) approach is that the TDC is mainly digital and the number of analog components in the analog-to-time converter is minimal; a simple sample and hold amplifier and a couple of comparators and a ramp generator. A ramp generator consisting of an inverter with a current source load driving a small capacitor provides sufficient accuracy. The approach offers the potential for low power, high speed and scalability with digital CMOS technologies as well as increased resolution as the sampling rate is lowered.

### Power Efficient Analog Circuits in CMOS

*Un-Ku Moon (Oregon State University)*

**Abstract** - Current research efforts are focused on developing new power efficient ADC architectures in recent CMOS processes. In the past year, a new power efficient  $\Delta\Sigma$  ADC was developed that is expected to yield both high resolution and wide signal bandwidth. Utilizing the extra order of noise-shaping characteristic that comes from the proposed two-step integrating quantizer, the  $\Delta\Sigma$  ADC manifests a third-order NTF (noise transfer function) with a second-order loop filter. The proposed ADC also incorporates a new feedback DAC topology that minimizes feedback DAC complexity in the context of the two-step multi-bit quantizer. In addition to our current research based on the two-step integrating quantizer, into the future we seek to also look into another power efficient ADC architecture suitable for high resolution and wide input bandwidth. Specifically, we would like to further explore the benefits of this two-step integrating quantizer and maximally explore the time based nature of such quantizer.

### An Ultra Low-Power PSK Transceiver for Wireless Sensing

*Brian Otis (University of Washington)*

**Abstract** - The focus of this project is the investigation of a very low power radio that does not sacrifice robustness or spectral efficiency. In my experience, low power radios that are actually in production fall into two categories: control radios (remote keyless entry, garage door, toys) and data radios (Zigbee, etc). The former are not robust and lack channelization and selectivity. The latter consume prohibitive amounts of power (>10mW). Our goal is to achieve both: extremely low cost and low power, but with the ability to robustly transmit data while providing channelization.

### Micro-Power Data Converters

*Gabor Temes (Oregon State University)*

**Abstract** – The purpose of the proposed research is to develop micro-power data converters, both ADCs and DACs. Micro-power A/D converters are often needed in sensor networks used for environmental monitoring, medical sensors and probes, industrial control, security and other

applications where power is provided by batteries or energy scavenging, and hence it is very limited. Micro-power DACs may be used in micro-stimulators and micro-actuators in biomedical applications. They represent an important market for the microelectronics industry. Under the proposed research, we shall continue the development of novel and efficient micro-power data converters, both analog-to-digital and digital-to-analog ones, which can be used in the most common biomedical and environmental applications.

### **Enabling Metal-Fill-Aware Design of RF/Mixed-Signal Integrated Circuits**

*Andreas Weisshaar (Oregon State University)*

**Abstract** - This project aims at (i) characterizing the performance degradation of RF circuits and components due to metal fill required in advanced IC processes, (ii) developing CAD algorithms to enable quick and accurate estimation of electromagnetic impact of metal fill, and (iii) providing RF/mixed-signal IC designers practical information, algorithms and tools. Our CAD algorithms will generate Spice/Spectre compatible lumped element equivalent circuit models for interconnects and spiral inductors including metal fill. This research will also directly help IC designers better understand the adverse impact of metal fill on RF circuits and help them to optimize their designs. Validation will include fabrication and measurement of representative test structures.