

## CDADIC RESEARCH TOPICS FY06

Below is a list of research topics of interest to CDADIC industry partners.

<b>CIRCUIT DESIGN</b>
Fractional n-synthesis on PLLs, with Low Jitter and Phase Noise
High-Resolution (>10 bits), High-Speed (>40 Ms/s), Low Latency (non-pipelined) ADCs in a Digital-Only CMOS Process. No capacitors
Design of Line Drivers for Wired Communication Systems: Low Distortion at Low Power to 10+ MHz (XDSL)
SiGe Design for WCDMA Front End
High-Speed, High SFDR DACs in <0.18 $\mu$ m Digital CMOS 90dB, 100MHz
Improved CMOS Bandgap Reference (<1% Absolute, <20ppm)
Bi-CMOS Optimized Mixed-Signal Designs
High-Speed (>10msps 14+ bits) ADC+DACs
Low-Phase Noise Submicron VCOs
High-Voltage Op Amps in Low-Voltage CMOS Processes
Low-Power, Low-Drift Precision References on Standard CMOS Processes
Continuous-Time Delta-Sigma Multi-Bit ADC/DACs
Low-Cost 5.6 GHz RF Circuits & Down Conversion Receivers
Micro-Power Biasing Techniques (on-chip sub 1uA, constant gm, etc.)
Adaptive Digital Error Cancellation in Data Converters
High-Performance Sample-and-Holds
Substrate Noise Coupling Models for Mixed-Signal Design
Micro-Power Data Converters (16+bits, 100uW, etc.)
Adaptive DSP Compensation for Analog Distortions in 2.4 & 5.8 GHz Transceivers
Precision ASIC Cells for Wide Temperature
Phased-Array Antenna Circuit Elements
Switched-Capacitor Circuits in Digital CMOS Technology
SiGe Data Acquisition Circuits up to 30GHz
RF Power Amps
RAD Hard CMOS Mixed-Signal Circuits Design
GaAs/InP ADC (250 MHz, 14-16 bits; 1gsp @ 12 effective bits)
High-Sensitivity Low-Noise CMOS Imagers
CMOS Imager Architectures for Very-High Resolution Arrays
Ultra-High Speed Digital Circuit Synthesis & Layout
Multiple Input – Multiple Output DC/DC Converters
Driving-Switched Cap Loads Quickly & Accurately at Low Power
High Dynamic Range Filters as in those used in IF Stages
Mixers with High Image Rejection (>30dB)
High IP3, Low-Voltage Supply CMOS Elements; Amps, Mixers, etc.
Ultra-Low Power Standard Analog Elements Designs
Ultra-Wideband 2-10.5 GHz Circuits
Reconfigurable Systems for Flexibility or for Self-Healing
Digital Beam Forming Methods for Phased-Array Antennas
Very High Speed Serializer - Deserializer
Sub 1Volt Supply Bandgap Reference
Capacitive Sensor Circuits
Substrate Noise Immune Circuit Topologies
Low Cost SiGe 11 - 15GHz LNA, PA, Switches, Attenuators
Ultra-Low Power Radio
1/f Noise Immune VCOs
Ultra Low Power Digital Circuits

Acoustic Charge Transport Devices or CCDs for Tunable HF High Q Filters

## **MODELING AND SIMULATION**

Integration of Substrate Noise Models with Industry Tools (practical implementation)

ESD Modeling for CMOS Plus Simulation Models

On-Chip Interconnect Models for High-Frequency/Speed Integrated Circuits on Silicon Substrate

Deep-Submicron Analog Layout Automation for Performance & Manufacturability

Simulation of Noise in Nonlinear Circuits

Behavior Modeling of RF Circuit Blocks & Development of RF Circuit Models

Analog CAD – Synthesis Methods

Universal Models for Device Stress & Failure Analysis

CMOS RF Power Transistors and Amplifiers Modeling & Simulation

Efficient Thermal Behavior of Packaged Integrated Circuit Devices

Efficient Mix-Mode Schematic Capture, Simulation and Layout

Sealable Modeling and Design of Embedded Passives

Analog Accurate and Characterizable MOS Models for Deep Sub-Micron with Open Access Hooks

Single Event Modeling and Mitigation Methods for Deep Sub-Micron

SiGe, and Trench SiGe Substrate Noise Coupling Over Frequency

Radiation Effects on 1/f Noise Both Modeling and Characterization

SOS Modeling

High Frequency Package Effects Modeling

MOS Noise Modeling in Different Operating Regions, HF Noise Modeling

## **TEST**

Test and Evaluation/Verification

Built in Analog and RF Self Testing

## **NEW TOPICS FOR FY06**

Sealable and Transportable Reliability Coupons

Fast Converging PLL

Adaptive Equalization for Line Drivers

Leakage Immune Analog Design

Multiple Voltage Range Analog on Low V CMOS

Accurate Models of Single Event Transients and Effects

Automated Single Event Analysis Tools

Low Phase Noise Logic Techniques

High Temp (200C) Analog Designs

Clockless Logic in Mixed Signal Comms

Tools for Predictive Design in Way Submicron Circuits

Novel Non-Volatile Memory for Rad Hard & Embedded Designs

Automatic Speed Power Optimization of Mixed Signal & RF Designs

Very High Dynamic Range Low Cost Circuits.

Modeling and Simulation of Lorentzian Noise in Ways Submicron CMOS